

Poster Abstract: A Modular Power-Aware Wireless Microsensor Architecture

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Categories and Subject Descriptors

C.3 [Special-Purpose and Application-Based Systems]: *Microprocessor/microcomputer applications, Real-time and embedded systems, Signal processing systems.* J.7 [Computers and Other Systems]: *Military.*

General Terms

Performance, Design, Standardization.

Keywords

Microsensor Architecture, Reconfigurable Systems, Distributed Systems.

1. INTRODUCTION

We introduce a modular power-aware wireless microsensor architecture targeted for unattended ground sensor applications. Typical ground sensor applications involve using a wide range of sensing modalities to track and identify the movements of people and vehicles in potentially hostile environments. In these settings where sensors are often battery-powered, power-awareness is an important metric to enable dynamic tradeoffs in sensing performance in exchange for longer sensor field lifetimes. For example, to conserve power within a particular sensor or sensor network operating at a low perceived threat level, a low-power acoustic signature detector may be run continuously. Meanwhile a higher-power video imager and processor may be activated only in response to sensor field alerts from either the acoustic detector or a remote source. At a higher perceived threat level, video surveillance might run continuously to improve detection, but at the cost of a shorter overall sensor field lifetime.

A modular sensor architecture is needed in these applications for two reasons: 1) Rapid physical reconfiguration with various communications links, and processing and sensing modalities is needed for rapid deployment in different mission scenarios, and 2) Dynamic in-the-field reconfiguration is needed to enable dynamic power consumption tradeoffs against overall sensor network performance. The central idea of this work is a decentralized

modular architecture in which each module is decoupled from a common continually-powered “main processor.” This enables properties of both rapid reconfiguration and power distribution to only the active sub-modules when needed.

A distributed/modular sensor architecture contrasts with the central processor approach used in many observed microsensor systems. In these systems, all sensors and communication systems are connected to a common processor which must be powered when any part of the system is active. Since the processor must be sized for the most power-intensive task expected, these systems are limited in their low-end processing capability. Conversely systems centered around a small-scale processor cannot scale up to high-end processing needs. A distributed architecture allows a single microsensor system to span both high and low-end application needs.

The highlight of the architecture is a dynamic system which can scale in performance over a 1000x range -- from very minor processing of less than 1 mW to significant processing requiring 1W or more. This poster describes initial results in converting a non power-aware acoustic tracking application to one which uses a distributed architecture. By isolating the main processor/CPU from the acoustic data collection process and from the RF communication link, significant power savings is achieved. Continuous sensing power is reduced from 196mW to 64mW in a vehicle-tracking scenario.

A “family” of interchangeable processor, radio, and sensor modules has been designed and built which includes: 1) a low-power microcontroller network for sub-module discovery and distributed sub-module power management, 2) independently switched serial channels (i2c, SPI, UART) for low-overhead module data interconnect, and 3) an optional high bandwidth processor bus for data intensive operation. The high-bandwidth processor module features a dynamic voltage scaling 400MHz Intel XScale PXA255 running Linux with 64MB SDRAM and 32MB FLASH and an SA1111 co-processor with USB master and Compact FLASH support. Because of the modular architecture, this processor can be completely shut off when it is unneeded.

2. ACKNOWLEDGEMENTS

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Power Aware Microsensor



- n Family of Interchangeable Modules
 - o Processor/Sensor/Radio, and Power.
- n Mix and Match
 - o Auto-reconfigurable through software discovery.
- n Mission Scalable
 - o 60-pin modules have 2°C power control bus and six switched serial channels (2xSPI, 2xI²C, & 2xUART).
 - o 180-pin modules add processor bus, (2) compact flash, USB master/slave, CD, and various GPIOs.

- n Tracker/Imager
 - o Radio Module
 - o Power/Battery
 - o Sensor + DSP
 - o FPGA/Imager
 - o Embedded Processor
 - o Compact Flash

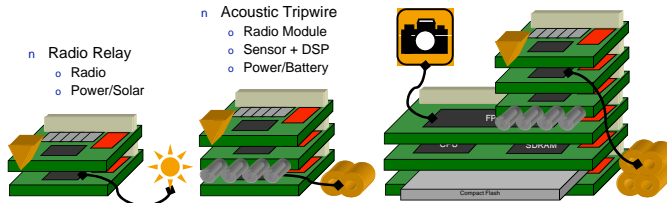
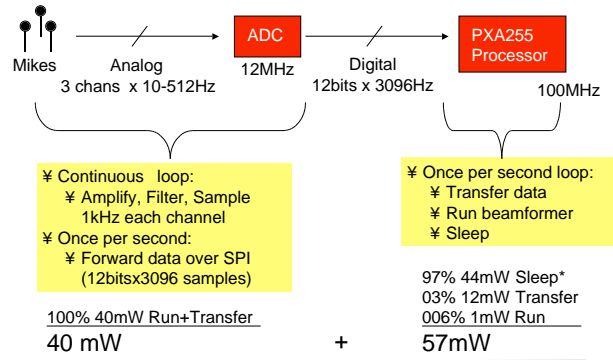


Figure 1 Modular Microsensor Family



12 Month Milestone Acoustic Beamformer < 100mW Budget



397mW End-to-End, June 20, 2003

* Expect < 11 mW after sleep s/w update = 64mW total

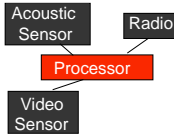
Figure 4 Power Reduction Status June 2003



Processor-Centric versus Distributed Architecture



Processor-Centric (motes, WINS) Pros and Cons



- (Power, Performance) Scalability is difficult
- Processor required for all transactions
- Processor must be sized for peak processing requirements
- + Easier to design with current COTS parts

Distributed (PASTA)



- + (Power, Performance) Scalability defines architecture
- + Distributed modules can act independently
- + Large processor Off/Asleep when unneeded
- Functions off-loaded to specific modules
- More complex design

Figure 2 Architecture Comparison



Example Architecture Comparison



Acoustic Processing Application



System Power (mW)

Processor-Centric Architecture	Distributed Architecture
Proc. idle 97% of time 150	7 Proc. asleep 97% of time
Processor Active 3% of time 10	10 Processor Active 3% of time
ADC active 100% of time 36	36 ADC active 100% of time
Total Power 196	43 Total Power

Ability to "sleep" processor cuts power by 75%

* Power estimates based on design-specification for PASTA PXA250 Processor module and 4-channel audio ADC subsystem. 12-month deliverable

Figure 3 Architecture Power Savings

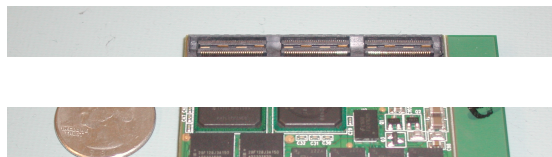


Figure 6 Photo of PXA processorboard

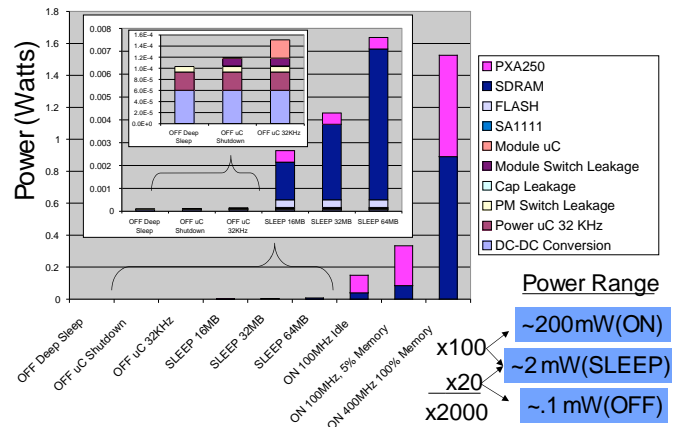


Figure 5 Power Range when Processor is On/Sleep/Off